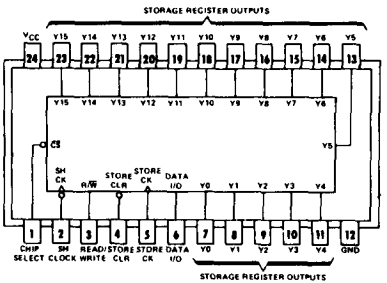
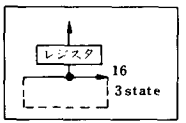
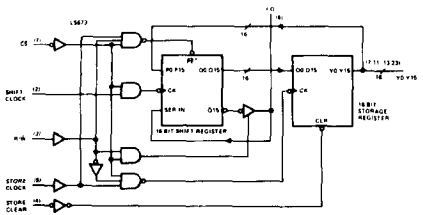
74673 16-Bit Shift Register



○シリアル → パラレル変換用





INPUTS					SERIAL	OPERATION
CHIP	SHIFT REG		STORAGE		I/O	
SELECT	R/$\overline{W}$	CLOCK	CLEAR	CLOCK	PORT	
X	L	X	L	X	Z	L input to ST CLR clears
H	X	X	L	X	Z	Storage registers; I/O depends
L	H	X	L	X	Q15	on $\overline{CS}$ and R/$\overline{W}$.
H	X	X	X	X	Z	No shifting or loading
L	L	↓	X	X	Z	Shift and write (load)
L	H	↓	X	L	Q14n	Shift and read
L	H	↓	L	H	L	Reload shift register from
L	H	↓	H	H	Y15n	storage, no shifting
L	L	X	H	↑	Z	Load storage from shift register

項目	大小	入力	IN	出力	OUT	N	LS	ALS	ALSK	F	S	AS	AC	ACT	HC	HCU	HCT	BC	BCT	単位
fmax	min	CLK					20			100					21					MHz
tw	min	CK, CLR					20			7					20					ns
tsu	min	I/O					20↓			3					25					ns
tsu	min	OTHERS					35↑			7					25					ns
thold	min	ALL					0↑			0					5					ns
tpd	max	ST-CLR		Y0～15			40			14					50					ns
tpd	max	ST-CLK		Y0～15			45			22					50					ns
tpd	max	SH-CLK		I/O			40			12.5					50					ns
tpd	max	CS, R/W	A	I/O			45			7					38					ns
tpd	max	CS, R/W	N	I/O			(40)			7					38					ns
Icc	max	Vc=MAX					80			160					0.04					mA
IIH	max	I/O					40			70										μA
IIL	max	I/O					0.4			0.6										mA
IIH	max	OTHERS	H				20			20										μA
IIL	max	OTHERS	L				0.4			0.6										mA
IOH	max			Y0～15	H		0.4			1					4					mA
IOL	max			Y0～15	L		8			20					4					mA
IOH	max			I/O	H		2.6			1					6					mA
IOL	max			I/O	L		24			20					6					mA
IZL	max			I/O	L		400								50					μA

社名	N	LS	ALS	ALSK	F	S	AS	AC	ACT	HC	HCU	HCT	BC	BCT
日立										D				
JRC														
MOT														
日電														
NS					F									
沖														
PHIL														
RCA														
三洋														
SIGNE														
TI		D												
東芝														